UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,254	01/02/2002	Roni Rosner	042390.P12485	9368

8791 7590 03/11/2004

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD, SEVENTH FLOOR
LOS ANGELES, CA 90025

EXAMINER	
KISS, ERIC B	

ART UNIT	PAPER NUMBER
2122	4

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	10/039,254	ROSNER ET AL.	
	Examiner	Art Unit	
	Eric B. Kiss	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2,3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-29 have been examined.

Drawings

2. The drawings are objected to because "PROCESSORS 102-104" in Fig. 1 should presumably be labeled --PROCESSORS 102, 104-- (or in any equivalent manner), as no *PROCESSOR 103* is referenced in the specification. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to because the multiple references to "functional units 212-218" in the specification (see, for example, p. 7, line 2) should instead refer to the illustrated functional units 212, 214, 216, and 218 (there are no illustrated functional units 213, 215, or 217 in Fig. 2). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: "314" in Fig. 3. A proposed drawing correction, corrected drawings, or amendment to the specification to add the

reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 27 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 27 recites the limitation "the instruction set architecture execution flags" in line 2. There is insufficient antecedent basis for this limitation in the claim. In the interest of compact prosecution, the above-mentioned limitation is subsequently interpreted as --and instruction set architecture execution flags-- for the purpose of further examination.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 7-9, 11, 12, 25, 28, and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No 5,802,373 to Yates et al.

As per claim 1, *Yates et al.* disclose receiving a binary of a program code, the binary based on a first instruction set architecture (see, for example, the Abstract); and translating the binary, wherein the translated binary is based on a combination of the first instruction set architecture and a second instruction set architecture (see, for example, the Abstract).

As per claim 7, *Yates et al.* further disclose the first instruction set architecture comprising floating-point instructions and wherein the second instruction set architecture comprises floating-point instructions, wherein the translating of the binary comprises translating the floating-point instructions of the first instruction set architecture to the floating-point instructions of the second instruction set architecture (see, for example, col. 47, lines 1-4).

As per claim 8, *Yates et al.* further disclose the translating of the binary comprising storing a portion of a hardware stack in a register of a processor translating the binary (see, for example, col. 46, lines 57-67).

As per claim 9, *Yates et al.* disclose receiving a binary of a program code, the binary based on a first instruction set architecture (see, for example, the Abstract); and executing the binary, wherein the executing comprises translating at least one instruction of the binary based on the first instruction set architecture to at least one instruction based on a second instruction set architecture (see, for example, the Abstract).

As per claim 11, *Yates et al.* further disclose, in the case of self modifying code, the translating of the binary to include an instruction to controllers of memories that store the binary to perform write operations independent of whether the write operations modify a location where the binary is stored (see, for example, col. 10, lines 49-53).

As per claim 12, *Yates et al.* further disclose the second instruction set architecture having an address space that is larger than the first instruction set architecture, the translating of the binary comprising using the address space of the second instruction set architecture (see, for example, col. 83, lines 56-65).

As per claims14 and 17, these are system versions of the claimed methods discussed above (claims 9 and 12, respectively). *Yates et al.* further disclose a system for implementing the prescribed methods (see, for example, Fig. 1), and all other limitations have been addressed as set forth above.

As per claims 25, 28, and 29, these are machine-readable medium versions of the claimed methods discussed above (claims 1, 7, and 11, respectively). *Yates et al.* further disclose the use of such a machine-readable medium for implementing the prescribed methods (see, for example, Fig. 1), and all other limitations have been addressed as set forth above.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No 5,802,373 to Yates et al. in view of Bich C. Le, "An Out-of-Order Execution Technique for Runtime Binary Translators," 1998 (hereinafter *Le*).

As per claim 10, in addition to the disclosure applied above to claim 9, *Yates et al.* fail to expressly disclose the first instruction set architecture including in-order access to memory and the second instruction set architecture including out-of-order accesses to memory, the translating of the binary to include out-of-order accesses to memory by a processor executing the binary. However, *Le* teaches a runtime binary translator environment which facilitates out-of-order processing in the translated code (see, for example, sections 1.1 and 1.2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of *Yates et al.* to include out-of-order accesses to memory as per the teachings of *Le*. One would be motivated to do so to achieve higher performance.

11. Claims 2-6, 13, 15, 16, 18-24, 26, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No 5,802,373 to Yates et al. in view of U.S. Patent No. 6,496,922 to Borrill.

As per claim 2, in addition to the disclosure applied above to claim 1, *Yates et al. fail* to expressly disclose checking instruction set architecture execution flags, the instruction set architecture execution flags to indicate at least one translation of a portion of the binary. However, *Borrill* teaches the use of instruction set architecture execution flags (an ISA tag) indicating the native ISA for "visiting" code (see, for example, col. 2, line 58, through col. 3, line 11; and col. 4, lines 30-58). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of *Yates et al.* to include such checking of instruction set architecture execution flags as per the teachings of *Borrill*. One would be motivated to do so to reduce overhead associated with translating and processing non-native instructions and facilitate easier incorporation of non-native instructions into executable code.

As per claim 3, in addition to the disclosure and teaching applied above to claim 2, *Borrill* further teaches the instruction set architecture execution flags being set by a programming environment of the binary (see, for example, col. 2, line 58, through col. 3, line 11; and col. 4, lines 30-58). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the method of *Yates et al.* to include such setting of architecture execution flags as per the further teachings of *Borrill*. One would be motivated to do so to assign meaningful instruction identifiers recognizable by the native system.

As per claim 4, in addition to the disclosure and teachings applied above to claim 2, *Borrill* further teaches a register in a processor translating the binary being to store the instruction set architecture execution flags (see, for example, col. 4, lines 15-29). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the method of *Yates et al.* to include such storing/processing of architecture execution flags as per the further teachings of *Borrill*. One would be motivated to do so to as a necessary means of implementing and executing such instructions.

As per claim 5, in addition to the disclosure and teachings applied above to claim 2, *Yates et al.* further disclose executing the translated binary (see, for example, the Abstract). Therefore, for reasons stated above, such a claim also would have been obvious.

As per claim 6, in addition to the disclosure and teachings applied above to claim 5, *Borrill* further teaches the translating and executing being based on a command, the instruction set architecture execution flags based on a number of command line flags associated with the command (see, for example, col. 2, line 58, through col. 3, line 11; and col. 4, lines 30-58). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the method of *Yates et al.* to include such command line flags as per the further teachings of *Borrill*. One would be motivated to do so to reduce overhead associated with translating and processing non-native instructions and facilitate easier incorporation of non-native instructions into executable code.

As per claim 13, in addition to the disclosure applied above to claim 12, *Yates et al.* fail to expressly disclose data accessed by the binary being stored in a single segment in memory and

wherein an offset value for translating a virtual address to a physical address for the data is not modified during execution of the binary. However, *Borrill* teaches such handling of non-native addressing without modifying the non-native offset address (see, for example, col. 6, line 64, through col. 7, line 24). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of *Yates et al.* to include such non-native offset address handling as per the teachings of *Borrill*. One would be motivated to do so to provide simplified support and proper emulation for non-native instructions relying on a smaller address space.

As per claims 15, 16, and 18, these are system versions of the claimed methods discussed above (see claims 4, 3, and 13, respectively). *Yates et al.* further disclose a system for implementing the prescribed methods (see, for example, Fig. 1), and all other limitations have been addressed as set forth above. Therefore, for reasons stated above, such claims also would have been obvious.

As per claims 19-24, these are apparatus versions of the claimed methods discussed above (see claims 4, 7, 8, and 11-13, respectively). *Yates et al.* further disclose an apparatus for implementing the prescribed methods (see, for example, Fig. 1), and all other limitations have been addressed as set forth above. Therefore, for reasons stated above, such claims also would have been obvious.

As per claims 26 and 27, these are machine-readable medium versions of the claimed methods discussed above (claims 5 and 6, respectively). *Yates et al.* further disclose the use of such a machine-readable medium for implementing the prescribed methods (see, for example, Fig. 1), and all other limitations have been addressed as set forth above. Therefore, for reasons stated above, such claims also would have been obvious.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Eric B. Kiss whose telephone number is (703) 305-7737. The Examiner can normally be reached on Tue. - Fri., 7:30 am - 5:00 pm. The Examiner can also be reached on alternate Mondays.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Tuan Dam, can be reached on (703) 305-4552. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBK /EBK
March 4, 2004

TUAN DAM
SUPERVISORY PATENT EXAMINER